

REMARKS

Applicant respectfully requests reconsideration of this application. Claims 1-8 were pending. No claims have been canceled. Claim 5 has been amended. New claims 9-10 have been added without introducing any new matter. Claims 1-10 are currently pending.

Claim 5 has been objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Accordingly, claim 5 has been amended to be in independent form, including substantially all of the limitations of its base claim and any intervening claims. Withdrawal of the objection is respectfully requested.

Claims 1-4 and 6-8 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,631,447 of Morioka ("Morioka"). Applicant respectfully traverses the rejection.

Claim 1 as amended includes a limitation of:

a memory management unit to implement a first cache-coherency mechanism or a second cache-coherency mechanism using the TLB according to *a property of an operating system* to be run by the processor.

(Claim 1; emphasis added)

In contrast, Morioka fails to disclose at least the above limitation. According to Morioka, the translation lookaside buffer holds *area limit attribute information*, which helps identify whether a cache coherence control is to be executed only for cache memories in one of the clusters or for every one of the cache memories throughout the system in response to an access request from any one of the processors (Morioka, col. 4,

ln. 61-67). Specifically, the area limit attribute information defines *an extent of cache coherency area* using two attributes to indicate whether it is a local cache coherency (LCC) or a global cache coherency (GCC) (Morioka, col. 10, ln. 13-27). The area limit attribute information in Morioka is not a *property of the operating system* (OS). For at least this reason, Morioka fails to anticipate claim 1. Withdrawal of the rejection is respectfully requested.

For the reason discussed above with respect to claim 1, claims 4 and 6 are not anticipated by Morioka. Withdrawal of the rejection is respectfully requested.

Claims 2-3 and 7-8 depend, directly or indirectly, from claims 1 and 6, respectively. Thus, for the reason discussed above with respect to claims 1 and 6, claims 2-3 and 7-8 are not anticipated by Morioka. Withdrawal of the rejection is respectfully requested.

New claim 9 recites:

... wherein the first cache coherency mode supports *memory attribute aliasing* and the second cache coherency mode does not support memory attribute aliasing.
(Claim 9; emphasis added)

As stated in the Office Action, the reference relied upon does not teach nor suggest a computer system which operates in a first or second cache coherency mode according to a property of the operating system, wherein the first cache coherency mode supports memory attribute aliasing and the second cache coherency mode does not support memory attribute aliasing (Office Action, pp. 4-5). Therefore, it is respectfully submitted that claim 9 is novel and patentable over the art of record for at least this reason. Allowance of claim 9 is earnestly solicited.

For at least the reason discussed above with respect to claim 9, new claim 10 is also novel and patentable over the art of record. Allowance of claim 10 is earnestly solicited.

CONCLUSION


Applicant respectfully submits that the objection and rejections have been overcome by the amendments and remarks, and that the pending claims are in condition for allowance. Accordingly, Applicant respectfully requests the objection and the rejections be withdrawn and the pending claims be allowed.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. If any other petition is necessary for consideration of this paper, it is hereby so petitioned.

If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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Chui-kiu Teresa Wong
Attorney for Applicant
Reg. No. 48,042

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025-1026
(408) 720-8300
(408) 720-8383